Hyunwon Chung

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INTERESTS   Parallel Computing, Reconfigurable architecture, CGRA (Coarse-Grained Reconfigurable Architecture), Dataflow Architecture, Low-power SoC, VLSI design

EDUCATION

University of Michigan, Ann Arbor
MS, PhD. in Electrical and Computer Engineering   Aug 2022 – Current

Korea University, Seoul
BS. in Electrical Engineering (Include 2-year military service)   Mar 2015 – Feb 2022

RESEARCH

Ultra Low-power Audio Compression Processor
Co-advisors: Prof. David Blaauw and Prof. Hun-Seok Kim
- Developed performance and power models for compressed neural network architectures targeting real-time audio compression acceleration
- Modeled energy and performance trade-offs across convolution operators by analyzing loop ordering, dataflow strategies, and on-chip buffer/SRAM sizing
- Performed architecture-level design space exploration of systolic arrays, evaluating array dimensions and microarchitectural variants to identify hardware configurations optimized for compressed models

PROWESS (Processor Reconfiguration for Wideband Sensor Systems)
Co-advisors: Prof. David Blaauw and Prof. Hun-Seok Kim
- Developed a streaming processor with a hardware kernel launcher enabling 10 ns runtime reconfiguration without CPU intervention
- Designed a dynamic scheduling unit for graph-based, data-dependent kernel execution under multi-channel RF workloads
- Taped out the processor in 28 nm CMOS and delivered up to 8.3× end-to-end performance improvement and 5× PE utilization via concurrent execution and speculative preloading
- Achieved 248.5 GFLOPS/mm² compute density and 1.67 TFLOPS/W energy efficiency in 28 nm CMOS

COCHON (Configurable Optical Communications via Heterogeneous-Processing Optimized Node)
Co-advisors: Prof. David Blaauw and Prof. Hun-Seok Kim
- Contributed to a 130 mm² heterogeneous processor integrating optical transceiver and receiver digital baseband for beyond-5G communication systems
- Led top-level physical design and multi-clock SoC integration, driving robust clock-domain crossing (CDC) architecture and interface timing closure across multiple asynchronous accelerator domains
- Successfully taped out end-to-end silicon in the GF 12 nm process, coordinating cross-team integration across accelerator, baseband, and SoC subsystems

DASH-SoC (Domain-Focused Advanced Software Reconfiguration Heterogeneous)
Co-advisors: Prof. David Blaauw and Prof. Hun-Seok Kim
- Contributed to the development of two accelerators under the DARPA-funded DASH project
- DAP (Domain Adaptive Processor)
  - Redesigned the DAP compute architecture from 16-bit to 32-bit datapath, significantly improving compute capability and performance
  - Implemented multi-kernel execution support to efficiently handle diverse communication workloads
  - Led physical design optimization, resolving routing congestion and improving timing closure and silicon efficiency
- Fully Reconfigurable Accelerator for FEC
  - Architected a flexible forward-error-correction processor supporting 3GPP LTE/5G, WiFi, and SDA OCT standards

- Integrated six FEC modes within a unified architecture, enabling high protocol adaptability with minimal area overhead

Automatic Peak Detection Algorithm based on Continuous Wavelet Transform

Advisors: Prof. Yogesh Gianchandani   University of Michigan
- Developed software and algorithm pipeline for multi-detector micro-GC chromatogram analysis
- Improved peak-detection and baseline-correction accuracy using CWT-based sparse feature extraction
- Co-authored publication accepted to Journal of Chromatography A (2024)

Low Power Accelerators for ML & Communication Systems

Advisor: Prof. Jongsun Park   Korea University
- Designed a DCT-based JPEG encoder/decoder architecture and synthesized the RTL in 65nm TSMC Technology
- Developed a low-power hardware implementation of a Viterbi decoder architecture
- Proposed an 8-bit fixed-point low-power accelerator for convolutional neural networks
- Designed a folded architecture for fully-connected layers to improve compute efficiency

PUBLICATION

Hyunwon Chung, Parin Senta, Jason Yu, Yukun Fang, Pierre Abillama, Kuan-Yu Chen, Ronald Dreslinski, David Blaauw, Hun-Seok Kim. "A 248.5 GFLOPS/mm2, 1.67 TFLOPS/W Streaming Processor with Hardware-Level Scheduling for Advanced Spectrum Sensing." Under review (2026).

Sanghyuck Moon, Ashfakh Huluvallay, **Hyunwon Chung**, Myeongsu Ko, Seokhyeon Jeong, Jungho Lee, Mohammad Khreishah, Jeongtaek Chang, Hung Do, Caitlyn Sutherland et al. "A 95.0 dB Dynamic Range Zero-Bias PV Light-to-Digital Converter for Seawater Monitoring with Single Point Calibration." Under review (2026).

Yufan Yue, Kuan-Yu Chen, Xiangdoing Wei, Tutu Ajayi, **Hyunwon Chung**, Ronald Dreslinski, David Blaauw, Hun-Seok Kim. "QFEC: A 9.97Gb/s Fully Configurable Quad-Mode Decoder for LDPC, Polar, Turbo, and Convolutional Codes." IEEE Transactions on Circuits and Systems I: Regular Papers (2026)

Jiahao Lin, H. Umut Suluhan, **Hyunwon Chung**, , Arindam Dutta, Anish Vipperla, Gerard Gubash, Jacob Holtom et al. "An Overview of Challenges and Requirements for Real-Time Spectrum Sensing in Modern RF Autonomy Systems." IEEE Design & Test (2025)

Xiangyu Zhao, Ryan Aridi, Jacob Hume, Swetha Subbiah, Xingqi Wu, **Hyunwon Chung**, Yutao Qin, and Yogesh B. Gianchandani. "Automatic peak detection algorithm based on continuous wavelet transform for complex chromatograms from multi-detector micro-scale gas chromatographs." Journal of Chromatography A (2024)

SELECTED PROJECTS

A Dynamic Quantized CNN Processor with Analog MAC Operations
- *EECS 627 course project at the University of Michigan*
- Designed analog MAC unit which includes digital to pulse converter, analog datapath, and flash ADC
- Proposed dynamic quantization method which allows each layer have different fixed points
- Post-quantization training and quantization-aware training are both used for 5-bit quantization, to get proper accuracy on MNIST and Cifar-10 dataset

16 bit Microprocessor with In-memory computing technology based on 6T SRAM architecture
- *EECS 427 course project at the University of Michigan*
- Developed 16-bit Microprocessor based on RISC-V ISA, which includes RF, ALU, Controller, Program Counter, Shifter, and IMEM/DMEM
- Designed customized 6T-SRAM based in-memory computing (IMC) module into 16-bit microprocessor

Custom Design Projects
- Implemented 128-bit Lightweight Encryption Algorithm (LEA) Decryption security module using Matlab & Verilog and synthesized it using 90nm TSMC technology
- Developed several circuit design including Inverter Chain, Ring Oscillator, SRAM, 3-tap FIR filter, and Flip-Flops. This includes the schematic, layout, and post-layout simulation

The World Embedded Software Contest - AI Humanoid Division
- Developed a program for real-time image processing and humanoid robot control using python

- Won 3rd place and Awarded Embedded SW & System Industry Association Chairman's award

Computer Architecture Project
- Developed Inverse-matrix program and heap-sort program using ARM assembly language
- Implemented TCP Server-Client program using multi-thread technique in C

SKILLS

Languages : C, C++, Verilog, SystemVerilog, Python, OpenMP, CUDA, PyTorch, Tensorflow
Hardware Simulation Tool : PSPICE, Design Complier, Model Sim, VCS
Circuit Design Software : Virtuoso, Innovus, Calibre

MILITARY SERVICE

Korean Augmentation To the United States Army,
Squad Leader, Sergeant, Headquarter, 23rd CBERN, 2ID, Camp Humphreys   Sep 2016 – Jun 2018

AWARDS & SCHOLARSHIPS

Electrical and Computer Engineering Department Graduate Fellowship, University of Michigan   2025
Dean's list at School of Electrical Engineering, Korea University   2018 - 2021
Miraero Scholarship at School of Electrical Engineering, Korea University   2016
National Scholarship (Admission with highest distinction), Korea University   2015